The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte LAERTIS ECONOMIKOS,
MUKTA S. FAROOQ, MICHAEL F. MCALLISTER,
ERIC D. PERFECTO, CHANDRIKA PRASAD,
KESHAV PRASAD, MADHAVAN SWAMINATHAN,
THOMAS A. WASSICK and GEORGE WHITE

_____

Appeal No. 1998-3071
Application 08/477,054

_____

ON BRIEF

_____

Before THOMAS, FLEMING and LALL, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

ON REQUEST FOR REHEARING

In a paper filed on April 26, 2001, bearing a Certificate of Mailing date of April 23, 2001, appellants request that we rehear our decision of February 23, 2001, in which we affirmed and reversed the rejection of some claims under 35 U.S.C. § 102 and affirmed

and reversed some claims rejected under 35 U.S.C. §103. The request is thus filed in a timely manner. In the request appellants set forth what amounts to three points alleging misapprehension by us in our earlier opinion of certain features of the prior art as applied only to independent claims 1, 15 and 24 on appeal, which are in the context only of the rejection within 35 U.S.C. § 102.

As to the first point, appellants allege that we improperly interpreted what constitutes a "chip site" in independent claims 1, 15 and 24. We do not see that appellants have alleged any error at pages 2-4 of the request. We discussed chip sites in various contexts at pages 6-9 of our original opinion even to the point of making reference to appellants' disclosure in the paragraph bridging pages 8 and 9 of our original opinion as the term was originally used in the specification as filed.

Appellants' reference to plural integrated circuit chips as discussed at page 3 of the request is noted. Besides stating that Sommerfeldt is consistent with appellants' consideration of what a chip site is, appellants make reference to their own specification generally relating to a discussion of Multi-Chip Modules or MCMs. The discussion at columns 1 and 2 of Sommerfeldt is consistent with this description of what an MCM is.

Thus, Sommerfeldt clearly suggests there, if not its entire discussion and the portions we outlined at pages 6-9 of our original opinion, that plural integrated circuit chips or plural chips may be embodied on the top surface of the Figure 1 device 10 in Sommerfeldt.

At the bottom of page 6 of our original decision, we stated that the "entire depiction in Figure 2 [of Sommerfeldt] may comprise a so-called ‘chip site.’ We therefore agree with the examiner’s view expressed at the seventh page of the answer." There, the examiner states that "any group of these pads can be called a chip site." It is appellants and not us or the examiner at page 2 of the request that indicates that only two bonding pads may constitute a chip site. Appellants’ discussion in the remaining portion of the first alleged error seems to be focused only upon a consideration of two bonding pads as a chip site. The examiner seemed to be indicating that Sommerfeldt’s chip sites may be located anywhere. It appears that appellants have attempted to set up a redherring argument only to shoot it down. We also indicated at the bottom of page 8 of our original opinion that appellants’ discussion of chip sites in the paragraph
bridging specification pages 7 and 8 should not be considered to be sites for receiving complete integrated circuits or chips themselves since they are merely described there to receive discrete semiconductor devices.

Appellants next assert at pages 4-6 of the request that we misapprehended "whether Sommerfeldt accomplishes their wiring objectives on a single sublayer as required by Appellants' claims 1, 15 and 24." Appellants state at the top of page 5 that "there is no teaching or disclosure in Sommerfeldt that one of the upper or lower planes may be used to the exclusion of the other." Appellants invite us at the top of page 6 "to particularly point out where in Sommerfeldt it is stated or disclosed that one of the upper or lower wiring planes may be used alone to connect wiring cells or route the conductive lines across the interconnect device."

At the outset, we noted at page 6 of our original opinion that the respective planes or layers 68 and 70 of representative Figure 8 and their corresponding layers in Figures 2, 3, and 6 may separately comprise an individual or single sublayer to the extent recited at the end of each independent claim 1, 15 and 24 on appeal. We remain of this view. The "comprising" nature of each independent claim 1, 15 and 24

on appeal does not exclude the fact that Sommerfeldt may require additional layers beyond the planes or layers 68 and 70 of representative Figure 8. Sommerfeldt's Figure 8 layers compare with appellants' layers in Figure 1 as disclosed. Moreover, Sommerfeldt

states at lines 3-6 of the abstract that the "interconnect device is fully customizable or programmable upon the upper surface to accommodate various electrical components and connectivity to those components." A similar statement is made in Sommerfeldt's Summary of the Invention at the bottom of column 2 at lines 64 and 65 which is that "the improved MCM hereof is not only fully programmable on only the surface layer." We identified certain layers in Sommerfeldt as comprising the claimed "single sublayer" in the last lines of each independent claim on appeal. These claims require nothing more.

Finally, we turn our attention to the third point at pages 6 and 7 of the request. There, appellants alleged that we misapprehended whether Sommerfeldt discloses the inter pad limitation of independent claims 1, 15 and 24. The context in which we discussed the inter pad spacing at the top of page 10 is the whole paragraph bridging pages 9 and 10. The basic premise is that the bonding pads may be connected in any manner in association with the use of connective links 58 shown in Figures 6 and 7. All of this is caught up in the context of what we considered to be a chip site as discussed in this paragraph. All that the claim requires is that a pair of connection pads at one chip site be separated from the chip connection pads at another site by a space greater than any of the

inter pad spaces. Because Sommerfeldt indicates that his integrated circuit chips may be mounted in various locations or "chip sites," the spacing between them implicitly is greater than any space between the pads themselves at least to provide enough space between the chip sites or the integrated circuit chips themselves.

Since we are unpersuaded that we misapprehended or overlooked appellants' three enumerated points as set forth in the request for rehearing, we do not change our views expressed in our February 23, 2001 opinion that the subject matter of independent claims 1, 15 and 24 was anticipated by Sommerfeldt within 35 U.S.C. § 102.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REHEARING DENIED

James D. Thomas Administrative Patent Judge	))))) BOARD OF PATENT
Michael R. Fleming Administrative Patent Judge	)) APPEALS AND)) INTERFERENCES
Parshotam S. Lall Administrative Patent Judge	))

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